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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Automated extraction of run-time parameterisable cores from programmable device configurations**
James-Roxby, P.; Guccione, S.A.;
Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on , 17-19 April 2000
Pages:153 - 161

[Abstract] [PDF Full-Text (724KB)] **IEEE CNF**

2 **Reconfigurable computing at Xilinx**
Guccione, S.A.;
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on , 4-6 Sept. 2001
Pages:102

[Abstract] [PDF Full-Text (35KB)] **IEEE CNF**

3 **GeneticFPGA: evolving stable circuits on mainstream FPGA devices**
Levi, D.; Guccione, S.A.;
Evolvable Hardware, 1999. Proceedings of the First NASA/DoD Workshop on , 19-21 July 1999
Pages:12 - 17

[Abstract] [PDF Full-Text (56KB)] **IEEE CNF**

4 **A data-parallel programming model for reconfigurable architectures**
Guccione, S.A.; Gonzalez, M.J.;
FPGAs for Custom Computing Machines, 1993. Proceedings. IEEE Workshop on , 5-7 April 1993
Pages:79 - 87

[Abstract] [PDF Full-Text (552KB)] **IEEE CNF**

Your search matched **1** documents.

A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **An evaluation of message passing implementations on Beowulf workstations**
Carns, P.H.; Ligon, W.B., III; McMillan, S.P.; Ross, R.B.;
Aerospace Conference, 1999. Proceedings. 1999 IEEE ,Volume: 5 , 6-13 March 1999
Pages:41 - 54 vol.5

[Abstract] [PDF Full-Text (652KB)] **IEEE CNF**

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A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Adapting constant multipliers in a neural network implementation**
James-Roxby, P.; Blodget, B.A.;
Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on , 17-19 April 2000
Pages:335 - 336

[Abstract] [PDF Full-Text (180KB)] **IEEE CNF**

2 **A lightweight approach for embedded reconfiguration of FPGAs**
Blodget, B.; McMillan, S.; Lysaght, P.;
Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003
Pages:399 - 400

[Abstract] [PDF Full-Text (KB)] **IEEE CNF**

3 **A high I/O reconfigurable crossbar switch**
Young, S.; Alfke, P.; Fewer, C.; McMillan, S.; Blodget, B.; Levi, D.;
Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003
Pages:3 - 10

[Abstract] [PDF Full-Text (3138KB)] **IEEE CNF**

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A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
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'configuration bitstream' <and> simulation Search

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Results Key:
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1 **A fault injection tool for SRAM-based FPGAs**
Alderighi, M.; D'Angelo, S.; Mancini, M.; Sechi, G.R.;
On-Line Testing Symposium, 2003. IOLTS 2003. 9th IEEE , 7-9 July 2003
Pages:129 - 133

[Abstract] [PDF Full-Text (342 KB)] **IEEE CNF**

2 **A tool for injecting SEU-like faults into the configuration control mechanism of Xilinx Virtex FPGAs**
Alderighi, M.; Casini, F.; D'Angelo, S.; Mancini, M.; Marmo, A.; Pastore, S.; Sechi, G.R.;
Defect and Fault Tolerance in VLSI Systems, 2003. Proceedings. 18th IEEE International Symposium on , 3-5 Nov. 2003
Pages:71 - 78

[Abstract] [PDF Full-Text (537 KB)] **IEEE CNF**

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A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

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fpga <and> (simulation <or> simulate) <and> object Search

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A maximum of **500** results are displayed, **50** to a page, sorted by **Publication year** in **Ascending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

config* and bitstream* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Multimedia teleconferencing over international packet switched networks**
Crowcroft, J.; Kirstein, P.T.; Timm, D.;
Communications Software, 1991, 'Communications for Distributed Applications and Systems', Proceedings of TRICOMM '91., IEEE Conference on , 18-19 April 1991
Pages:23 - 33

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

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2 **A fully integrated bitstream analogue-to-digital converter for digital audio**
Glover, M.; Hermes, B.; Kup, B.; Slowgrove, D.;
Analogue to Digital and Digital to Analogue Conversion, 1991., International Conference on , 17-19 Sep 1991
Pages:165 - 169

[Abstract] [PDF Full-Text (244 KB)] **IEE CNF**

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3 **The software radio architecture**
Mitola, J.;
Communications Magazine, IEEE , Volume: 33 , Issue: 5 , May 1995
Pages:26 - 38

[Abstract] [PDF Full-Text (1096 KB)] **IEEE JNL**

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4 **FPGA based runtime configurable clause evaluator for SAT problems**
Leong, P.H.W.; Chung, C.K.;
Electronics Letters , Volume: 35 , Issue: 19 , 16 Sept. 1999
Pages:1618 - 1619

[Abstract] [PDF Full-Text (280 KB)] **IEE JNL**

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5 **New implementation techniques of a real-time MPEG-2 audio encoding system**
Hyen-O Oh; Sung-Youn Kim; Dae-Hee Youn; Il-Whan Cha;
Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1999 IEEE International Conference on , Volume: 4 , 15-19 March 1999
Pages:2287 - 2290 vol.4

[Abstract] [PDF Full-Text (324 KB)] **IEEE CNF**

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6 **Lossless JBIG2 coding performance**
Tompkins, D.A.D.; Kossentini, F.;
Data Compression Conference, 1999. Proceedings. DCC '99 , 29-31 March 1999
Pages:553

[Abstract] [PDF Full-Text (8 KB)] **IEEE CNF**

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7 **GeneticFPGA: evolving stable circuits on mainstream FPGA devices**
Levi, D.; Guccione, S.A.;
Evolvable Hardware, 1999. Proceedings of the First NASA/DoD Workshop on , 19-21 July 1999
Pages:12 - 17

[Abstract] [PDF Full-Text (56 KB)] **IEEE CNF**

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8 **Encoding and reconstruction of incomplete 3-D video objects**
Ekmekci, S.;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 10 , Issue: 7 , Oct. 2000
Pages:1198 - 1207

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

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9 **Automated extraction of run-time parameterisable cores from programmable device configurations**
James-Roxby, P.; Guccione, S.A.;
Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on , 17-19 April 2000
Pages:153 - 161

[Abstract] [PDF Full-Text (724 KB)] **IEEE CNF**

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10 **High performance DES encryption in Virtex™ FPGAs using JBits™**
Patterson, C.;
Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on , 17-19 April 2000
Pages:113 - 121

[Abstract] [PDF Full-Text (712 KB)] **IEEE CNF**

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11 **A run-time reconfigurable plug-in for the Winamp MP3 player**
Scalera, J.; Jones, M.;
Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on , 17-19 April 2000

Pages:319 - 320

[Abstract] [PDF Full-Text (180 KB)] **IEEE CNF**

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12 **Influence of encoder parameters on the decoded video quality for MPEG-4 over W-CDMA mobile networks**
Soares, L.D.; Adachi, S.; Pereira, F.;
Image Processing, 2000. Proceedings. 2000 International Conference on , Volume: 2 , 10-13 Sept. 2000
Pages:148 - 151 vol.2

[Abstract] [PDF Full-Text (452 KB)] **IEEE CNF**

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13 **An architecture and implementation of MPEG audio layer III decoder using dual-core DSP**
Kyu Ha Lee; Keun-Sup Lee; Tae-Hoon Hwang; Young-Cheol Park; Dae Hee Youn;
Consumer Electronics, IEEE Transactions on , Volume: 47 , Issue: 4 , Nov. 2001
Pages:928 - 933

[Abstract] [PDF Full-Text (587 KB)] **IEEE JNL**

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14 **In-system reconfiguring and I^2C controlling of FPGA based applications**
Szymanski, T.; Kielbik, R.; Napieralski, A.;
CAD Systems in Microelectronics, 2001. CADSM 2001. Proceedings of the 6th International Conference. The Experience of Designing and Application of , 12-17 Feb. 2001
Pages:230 - 231

[Abstract] [PDF Full-Text (124 KB)] **IEEE CNF**

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15 **A format-compliant configurable encryption framework for access control of multimedia**
Jiangtao Wen; Severa, M.; Wenjun Zeng; Luttrell, M.; Weiyin Jin;
Multimedia Signal Processing, 2001 IEEE Fourth Workshop on , 3-5 Oct. 2001
Pages:435 - 440

[Abstract] [PDF Full-Text (499 KB)] **IEEE CNF**

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16 **Heavy ion characterization of SEU mitigation methods for the Virtex FPGA**
Sturesson, F.; Mattsson, S.; Carmichael, C.; Harboe-Sorensen, R.;
Radiation and Its Effects on Components and Systems, 2001. 6th European Conference on , 10-14 Sept. 2001
Pages:285 - 291

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

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17 **A reconfigurable architecture for a class of digital signal/image processing applications**
Sinha, A.; Karmakar, A.; Maiti, K.; Halder, P.;
Communications, Computers and signal Processing, 2001. PACRIM. 2001 IEEE Pacific Rim Conference on , Volume: 1 , 26-28 Aug. 2001
Pages:71 - 74 vol.1

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

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18 **Huffman code based error screening and channel code optimization for error concealment in perceptual audio coding (PAC) algorithms**
Laneman, J.N.; Sundberg, C.-E.W.; Faller, C.;
Broadcasting, IEEE Transactions on , Volume: 48 , Issue: 3 , Sept. 2002
Pages:193 - 206

[Abstract] [PDF Full-Text (456 KB)] **IEEE JNL**

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19 **A format-compliant configurable encryption framework for access control of video**
Jiangtao Wen; Severa, M.; Wenjun Zeng; Luttrell, M.H.; Weiyin Jin;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 12 , Issue: 6 , June 2002
Pages:545 - 557

[Abstract] [PDF Full-Text (394 KB)] **IEEE JNL**

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20 **Reconfigurable systems: A generalization of reconfigurable computational strategies for space systems**
Lyke, J.;
Aerospace Conference Proceedings, 2002. IEEE , Volume: 4 , 9-16 March 2002
Pages:4-1935 - 4-1950 vol.4

[Abstract] [PDF Full-Text (1755 KB)] **IEEE CNF**

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21 **Accelerator validation of an FPGA SEU simulator**
Johnson, E.; Caffrey, M.; Graham, P.; Rollins, N.; Wirthlin, M.;
Nuclear Science, IEEE Transactions on , Volume: 50 , Issue: 6 , Dec. 2003
Pages:2147 - 2157

[Abstract] [PDF Full-Text (1369 KB)] **IEEE JNL**

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22 **Fault injection into SRAM-based FPGAs for the analysis of SEU effects**
Asadi, G.; Miremadi, S.G.; Zarandi, H.R.; Ejlali, A.;
Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE International Conference on , 15-17 Dec. 2003
Pages:428 - 430

[Abstract] [PDF Full-Text (314 KB)] **IEEE CNF**

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23 **A tool for injecting SEU-like faults into the configuration control mechanism of Xilinx Virtex FPGAs**
Alderighi, M.; Casini, F.; D'Angelo, S.; Mancini, M.; Marmo, A.; Pastore, S.; Sechi, G.R.;
Defect and Fault Tolerance in VLSI Systems, 2003. Proceedings. 18th IEEE International Symposium on , 3-5 Nov. 2003
Pages:71 - 78

[Abstract] [PDF Full-Text (537 KB)] **IEEE CNF**

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24 **A fault injection tool for SRAM-based FPGAs**
Alderighi, M.; D'Angelo, S.; Mancini, M.; Sechi, G.R.;
On-Line Testing Symposium, 2003. IOLTS 2003. 9th IEEE , 7-9 July 2003
Pages:129 - 133

[Abstract] [PDF Full-Text (342 KB)] **IEEE CNF**

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25 **Transmission of block turbo coded digital audio over FM-SCA**
Janakiraman, V.; Jeen Sang Jang; Junghwan Kim;
Broadcasting, IEEE Transactions on , Volume: 50 , Issue: 2 , June 2004
Pages:107 - 112

[Abstract] [PDF Full-Text (208 KB)] **IEEE JNL**

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26 **Configuration bitstream compression for dynamically reconfigurable FPGAs**
Ju Hwa Pan; Mitra, T.; Weng-Fai Wong;
Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on , Nov. 7-11, 2004
Pages:766 - 773

[Abstract] [PDF Full-Text (879 KB)] **IEEE CNF**

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27 **Real-time configuration code decompression for dynamic FPGA self-reconfiguration**
Huebner, M.; Ullmann, M.; Weissel, F.; Becker, J.;
Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International , 26-30 April 2004
Pages:138

[Abstract] [PDF Full-Text (1368 KB)] **IEEE CNF**

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28 **An alternate wire database for Xilinx FPGAs**
Steiner, N.; Athanas, P.;
Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th Annual IEEE Symposium on , 20-23 April 2004
Pages:336 - 337

[Abstract] [PDF Full-Text (88 KB)] **IEEE CNF**

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29 **Dynamically configurable security for SRAM FPGA bitstreams**
Bossuet, L.; Gogniat, G.; Burleson, W.;
Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International , 26-30 April 2004
Pages:146

[Abstract] [PDF Full-Text (1363 KB)] **IEEE CNF**

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30 **QME: an efficient subsampling-based block matching algorithm for motion estimation**
Kun-Bin Lee; Hao-Yun Chin; Hui-Cheng Hsu; Chein-Wei Jen;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 2 , 23-26 May 2004
Pages:II - 305-8 Vol.2

[Abstract] [PDF Full-Text (297 KB)] **IEEE CNF**

31 **Evaluation of fault-tolerant designs implemented on SRAM-based FPGAs**
Asadi, G.; Miremadi, S.G.; Zarandi, H.R.; Ejlali, A.;
Dependable Computing, 2004. Proceedings. 10th IEEE Pacific Rim International Symposium on , 3-5 March 2004
Pages:327 - 332

[Abstract] [PDF Full-Text (247 KB)] **IEEE CNF**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"6430736".pn.	USPAT	OR	OFF	2005/02/14 10:01
L2	4	(6430736|6539532|6363517|6363519).pn.	USPAT	OR	OFF	2005/02/14 10:07
L3	5	(6668237|6665766|6557156|6144933|6212650).pn.	USPAT	OR	OFF	2005/02/14 10:08
L4	221	(configuration adj bitstream)	US-PGPUB; USPAT	OR	OFF	2005/02/14 10:12
L5	63	L4 and simulat$3	US-PGPUB; USPAT	OR	OFF	2005/02/14 10:12
S1	1	"6466898".pn.	USPAT	OR	OFF	2005/02/10 11:09
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S3	8	S2 not xilinx$.as.	US-PGPUB; USPAT	OR	OFF	2005/02/10 11:11
S4	1028	703/14,17,20.ccls.	US-PGPUB; USPAT	OR	OFF	2005/02/10 11:18
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S7	3	S6 and event	US-PGPUB; USPAT	OR	OFF	2005/02/10 11:21
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S10	221	(configuration adj bitstream)	US-PGPUB; USPAT	OR	OFF	2005/02/10 11:27
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	U	1	Document ID	Issue Date	Pages	Title
1	X		US 20040260528 A1	20041223	10	Co-simulation via boundary scan interface
2	X		US 20040216081 A1	20041028	29	Application-specific testing methods for programmable logic devices
3	X		US 20040196065 A1	20041007	18	Programmable devices with convertibility to customizable devices
4	X		US 20040167686 A1	20040826	11	Condition monitoring system
5	X		US 20040155684 A1	20040812	25	Multi-purpose digital frequency synthesizer circuit for a programmable logic device
6	X		US 20040088691 A1	20040506	63	Debugging and performance profiling using control-dataflow graph representations with reconfigurable hardware emulation
7	X		US 20040088689 A1	20040506	64	System and method for converting control flow graph representations to control-dataflow graph representations
8	X		US 20040088685 A1	20040506	64	Process for converting programs in high-level programming languages to a unified executable for hybrid computing platforms
9	X		US 20040088666 A1	20040506	63	System and method for partitioning control-dataflow graph representations
10	X		US 20040060032 A1	20040325	26	Automated system for designing and developing field programmable gate arrays

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
1	703/14			Ballagh, Jonathan B. et al.					
2	716/18	713/1; 713/100; 716/16; 716/4		Wells, Robert W. et al.					
3	326/41			Madurawe, Raminda Udaya					
4	701/19			Baker, Stephen et al.					
5	327/115	713/500		Nguyen, Andy T.					
6	717/158	717/134; 717/135		Hammes, Jeffrey et al.					
7	717/154	717/140; 717/155		Hammes, Jeffrey					
8	717/140	717/107; 717/121		Poznanovic, Daniel et al.					
9	716/7			Poznanovic, Daniel et al.					
10	716/16	716/17		McCubbrey, David L.					

	4	5	Image Doc. Displayed	PT
1			US 20040260528	
2			US 20040216081	
3			US 20040196065	
4			US 20040167686	
5			US 20040155684	
6			US 20040088691	
7			US 20040088689	
8			US 20040088685	
9			US 20040088666	
10			US 20040060032	

	U	1	Document ID	Issue Date	Pages	Title
11	X		US 20040049672 A1	20040311	31	System and method for hardware-software multitasking on a reconfigurable computing platform
12	X		US 20040004496 A1	20040108	18	Field programmable gate array with convertibility to application specific integrated circuit
13	X		US 20030107415 A1	20030612	26	Multi-purpose digital frequency synthesizer circuit for a proprammable logic device
14	X		US 20020174266 A1	20021121	12	Parameterized application programming interface for reconfigurable computing systems
15	X		US 20020010853 A1	20020124	88	Method of time multiplexing a programmable logic device
16	X		US 20010047509 A1	20011129	28	Modular design method and system for programmable logic devices
17	X		US 20010001881 A1	20010524	37	Methods and media for utilizing symbolic expressions in circuit modules
18	X		US 6817006 B1	20041109	28	Application-specific testing methods for programmable logic devices
19	X		US 6817005 B2	20041109	26	Modular design method and system for programmable logic devices
20	X		US 6802026 B1	20041005	8	Parameterizable and reconfigurable debugger core generators

21	X		US 6747478 B2	20040608	17	Field programmable gate array with convertibility to application specific integrated circuit

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
11	713/100			Nollet, Vincent et al.					
12	326/39			Madurawe, Raminda U.					
13	327/115			Nguyen, Andy T.					
14	719/328			Palem, Krishna et al.					
15	713/1	713/100; 713/501; 713/600		Trimberger, Stephen M. et al.					
16	716/18	716/7		Mason, Jeffrey M. et al.					
17	716/1	716/12; 716/13; 716/14		Mohan, Sundararajarao et al.					
18	716/16	716/17; 716/18		Wells; Robert W. et al.					
19	716/16	716/7; 716/8		Mason; Jeffrey M. et al.					
20	714/35	712/227		Patterson; Cameron D. et al.					

21	326/39	326/101; 326/47		Madurawe; Raminda U.					

	4	5	Image Doc. Displayed	PT
11			US 20040049672	
12			US 20040004496	
13			US 20030107415	
14			US 20020174266	
15			US 20020010853	
16			US 20010047509	
17			US 20010001881	
18			US 6817006	
19			US 6817005	
20			US 6802026	

21			US 6747478	

	U	1	Document ID	Issue Date	Pages	Title
22	X		US 6744816 B1	20040601	10	Video coding and decoding methods
23	X		US 6714057 B2	20040330	25	Multi-purpose digital frequency synthesizer circuit for a programmable logic device
24	X		US 6711674 B1	20040323	11	Method of watermarking configuration data in an FPGA by embedding the watermark corresponding to a macro obtained upon encountering a first watermark tag from the macro
25	X		US 6678646 B1	20040113	12	Method for implementing a physical design for a dynamically reconfigurable logic circuit
26	X		US 6651238 B1	20031118	21	Providing fault coverage of interconnect in an FPGA
27	X		US 6600788 B1	20030729	17	Narrow-band filter including sigma-delta modulator implemented in a programmable logic device
28	X		US 6594610 B1	20030715	11	Fault emulation testing of programmable logic devices
29	X		US 6510548 B1	20030121	9	Method for providing pre-designed modules for programmable logic devices

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
22	375/240			Park; Dong-seek et al.					
23	327/115	327/117; 377/47		Nguyen; Andy T.					
24	713/1	713/100; 713/168; 713/176; 713/2		Burnham; James L.					
25	703/22	703/24; 703/25; 716/5; 716/7; 716/8		McConnell; David A. et al.					
26	716/16	716/17; 716/4; 716/5		Wells; Robert W. et al.					
27	375/245	375/232; 375/243; 375/247		Dick; Christopher H. et al.					
28	702/117	702/123; 702/183; 702/58; 703/14; 703/27; 714/2; 714/30; 714/39; 714/725; 716/17; 716/4		Toutounchi; Shahin et al.					
29	716/16	716/17		Squires; David B.					

	4	5	Image Doc. Displayed	PT
22			US 6744816	
23			US 6714057	
24			US 6711674	
25			US 6678646	
26			US 6651238	
27			US 6600788	
28			US 6594610	
29			US 6510548	

	U	1	Document ID	Issue Date	Pages	Title
30	X		US 6510547 B1	20030121	8	Method and apparatus for evolving an object using simulated annealing and genetic processing techniques
31	X		US 6487648 B1	20021126	20	SDRAM controller implemented in a PLD
32	X		US 6480954 B2	20021112	86	Method of time multiplexing a programmable logic device
33	X		US 6457164 B1	20020924	38	Hetergeneous method for determining module placement in FPGAs
34	X		US 6453456 B1	20020917	12	System and method for interactive implementation and testing of logic cores on a programmable logic device
35	X		US 6351143 B1	20020226	15	Content-addressable memory implemented using programmable logic
36	X		US 6305005 B1	20011016	10	Methods to securely configure an FPGA using encrypted macros
37	X		US 6301695 B1	20011009	9	Methods to securely configure an FPGA using macro markers
38	X		US 6292925 B1	20010918	38	Context-sensitive self implementing modules
39	X		US 6278289 B1	20010821	14	Content-addressable memory implemented using programmable logic

40	X		US 6263430 B1	20010717	86	Method of time multiplexing a programmable logic device

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
30	716/16	345/419; 700/103; 706/13; 709/203		Levi; Delon					
31	711/167	326/39; 713/400; 713/503; 716/16		Hassoun; Joseph H.					
32	713/1	713/100; 713/501; 713/600		Trimberger; Stephen M. et al.					
33	716/8	716/10; 716/16; 716/18; 716/9		Hwang; L. James et al.					
34	716/16	716/17		Price; Timothy O.					
35	326/40	365/49; 711/108		Guccione; Steven A. et al.					
36	716/16	713/1; 713/100; 713/202; 716/18		Burnham; James L.					
37	716/16	713/1; 713/100; 716/17		Burnham; James L. et al.					
38	716/8	716/10; 716/14; 716/17; 716/2; 716/9; 719/315		Dellinger; Eric F. et al.					
39	326/40	326/39; 326/41		Guccione; Steven A. et al.					

40	713/1	713/100; 713/501; 713/600		Trimberger; Stephen M. et al.					

	4	5	Image Doc. Displayed	PT
30			US 6510547	
31			US 6487648	
32			US 6480954	
33			US 6457164	
34			US 6453456	
35			US 6351143	
36			US 6305005	
37			US 6301695	
38			US 6292925	
39			US 6278289	

40			US 6263430	

	U	1	Document ID	Issue Date	Pages	Title
41	X		US 6260182 B1	20010710	37	Method for specifying routing in a logic module by direct module communication
42	X		US 6243851 B1	20010605	37	Heterogeneous method for determining module placement in FPGAs
43	X		US 6216258 B1	20010410	39	FPGA modules parameterized by expressions
44	X		US 6212650 B1	20010403	11	Interactive dubug tool for programmable circuits
45	X		US 6144933 A	20001107	12	Method and apparatus for remotely probing and stimulating a programmable logic device
46	X		US 6011663 A	20000104	165	Digital VTR increasing recorded amount of high priority data
47	X		US 5995744 A	19991130	11	Network configuration of programmable circuits
48	X		US 5978260 A	19991102	89	Method of time multiplexing a programmable logic device
49	X		US 5959881 A	19990928	85	Programmable logic device including configuration data or user data memory slices
50	X		US 5838954 A	19981117	85	Computer-implemented method of optimizing a time multiplexed programmable logic device

51	X		US 5825662 A	19981020	85	Computer-implemented method of optimizing a time multiplexed programmable logic device

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
41	716/12	716/13; 716/14; 716/16		Mohan; Sundararajarao et al.					
42	716/10	716/1; 716/16; 716/17; 716/18; 716/21; 716/8; 716/9; 717/116; 717/118		Hwang; L. James et al.					
43	716/17	716/16; 716/18		Mohan; Sundararajarao et al.					
44	714/32	714/31; 714/38		Guccione; Steven A.					
45	703/23	703/28		Guccione; Steven A.					
46	360/48	386/109; 386/68; 386/73		Inoue; Sadayuki et al.					
47	703/23	713/100; 717/176		Guccione; Steven A.					
48	365/182	365/189.01		Trimberger; Stephen M. et al.					
49	365/182	365/51; 365/63		Trimberger; Stephen M. et al.					
50	716/16			Trimberger; Stephen M.					

51	716/3	326/39; 326/40; 716/16		Trimberger; Stephen M.					

	4	5	Image Doc. Displayed	PT
41			US 6260182	
42			US 6243851	
43			US 6216258	
44			US 6212650	
45			US 6144933	
46			US 6011663	
47			US 5995744	
48			US 5978260	
49			US 5959881	
50			US 5838954	

51			US 5825662	

	U	1	Document ID	Issue Date	Pages	Title
52	X		US 5787007 A	19980728	9	Structure and method for loading RAM data within a programmable logic device
53	X		US 5784313 A	19980721	86	Programmable logic device including configuration data or user data memory slices
54	X		US 5778439 A	19980707	85	Programmable logic device with hierarchical confiquration and state storage
55	X		US 5761484 A	19980602	17	Virtual interconnections for reconfigurable logic systems
56	X		US 5761483 A	19980602	85	Optimizing and operating a time multiplexed programmable logic device
57	X		US 5701441 A	19971223	85	Computer-implemented method of optimizing a design in a time multiplexed programmable logic device
58	X		US 5646545 A	19970708	89	Time multiplexed programmable logic device
59	X		US 5629637 A	19970513	87	Method of time multiplexing a programmable logic device
60	X		US 5600263 A	19970204	85	Configuration modes for a time multiplexed programmable logic device
61	X		US 5596742 A	19970121	15	Virtual interconnections for reconfigurable logic systems
62	X		US 5583450 A	19961210	88	Sequencer for a time multiplexed programmable logic device

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52	716/16	326/39; 326/41; 703/23		Bauer; Trevor J.					
53	365/182	365/156		Trimberger; Stephen M. et al.					
54	711/153	711/117; 711/156; 711/173		Trimberger; Stephen M. et al.					
55	716/16			Agarwal; Anant et al.					
56	716/2	326/40; 326/41		Trimberger; Stephen M.					
57	716/16	326/39; 326/41		Trimberger; Stephen M.					
58	326/38	326/40		Trimberger; Stephen M. et al.					
59	326/93	326/38; 326/46		Trimberger; Stephen M. et al.					
60	326/39	326/41; 326/93		Trimberger; Stephen M. et al.					
61	716/16			Agarwal; Anant et al.					
62	326/41	326/40; 326/93		Trimberger; Stephen M. et al.					

	4	5	Image Doc. Displayed	PT
52			US 5787007	
53			US 5784313	
54			US 5778439	
55			US 5761484	
56			US 5761483	
57			US 5701441	
58			US 5646545	
59			US 5629637	
60			US 5600263	
61			US 5596742	
62			US 5583450	

	U	1	Document ID	Issue Date	Pages	Title
63	X		US 5068603 A	19911126	68	Structure and method for producing mask-programmed integrated circuits which are pin compatible substitutes for memory-configured logic arrays

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
63	714/726	257/E23.151 ; 257/E27.105		Mahoney; John E.					

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63			US 5068603	